# SILICON-ON-INSULATOR WAFER FOR RF INTEGRATED CIRCUIT

## Technical Field of the Invention

The present invention relates to silicon-on-insulator (SOI) wafers for RF integrated circuits.

## Background of the Invention

The material requirements for the initial processing of the silicon used in a particular application are driven by that application. For RF applications, these material requirements are very stringent. Standard bulk silicon wafers or silicon-on-insulator wafers use low resistivity substrates that result in high losses and cross-talk at high frequencies. For example, the Q's of inductors fabricated using silicon wafers or silicon-on-insulator wafers having low resistivity substrates are low. Therefore, multi-level metals with a ground plane are used in order to achieve higher Q's. However, these coupling techniques result in cross-talk. In addition, losses increase at higher frequencies due to the low resistivity of the substrates.

Losses and coupling (cross-talk) in RF applications may be reduced by using high resistivity silicon (HRS) substrates. Such substrates have maximum resistivities $\rho$ of $10^4$ $\Omega$-cm as compared to a resistivity

$\rho$ of about 10 $\Omega$-cm for the silicon substrate typically used. However, the resistivity of HRS is 3-4 orders of magnitude lower than a GaAs substrate commonly used for RF applications. In addition, there is a problem with using high resistivity silicon substrates in RF applications. That is, during post-processing, thermally generated donors degrade the resistivity both at the $SiO_2$/Si interface and at the back of the wafer, as shown by the graphs in Figures 1 and 2.

Figure 1 is a resistance profile at the interface between the buried oxide and the substrate (i.e., the $SiO_2$/Si interface) where the substrate is assumed to be an n-type substrate. The y-axis of Figure 1 represents resistivity, and the x-axis represents depth into the substrate. The point at which x = 0 is at the interface. As shown in Figure 1, the resistivity of the substrate is lowest just below the interface.

Figure 2 is a resistance profile across a p-type wafer. The y-axis of Figure 2 represents resistivity, and the x-axis represents depth into the wafer. The point at which x = 0 is at the front surface of the wafer. As shown in Figure 2, the back of the wafer, under certain conditions, may actually undergo a

conversion in type (in this case, from p type to n type). It has also been observed that, under other conditions, the region of the wafer just below the buried oxide may also undergo a conversion in type.

The degradation at the back of the wafer may be removed by grinding. However, the degradation at the interface produces higher losses, increases coupling (cross-talk), lowers inductor Q, and is not so easily remedied. The present invention solves one or more of these problems

Summary of the Invention

In accordance with one aspect of the present invention, an RF semiconductor device comprises a high resistivity polysilicon handle wafer, a buried oxide layer over the polysilicon handle wafer, and a silicon layer over the buried oxide layer.

In accordance with another aspect of the present invention, an RF semiconductor device comprises a high resistivity polycrystalline layer, a buried oxide layer over the polycrystalline layer, and a silicon layer over the buried oxide layer.

In accordance with still another aspect of the present invention, a method of fabricating an RF semiconductor device comprises the following: forming an oxide layer on a surface of a first wafer, wherein the first wafer comprises low resistivity silicon; and, bonding the oxide layer of the first wafer to a second wafer, wherein the second wafer comprises a high resistivity polysilicon wafer, whereby the RF semiconductor device is produced.

In accordance with yet another aspect of the present invention, a method of fabricating an RF semiconductor device comprises the following: forming a first oxide layer on a surface of a first wafer, wherein the first wafer comprises a high resistivity polycrystalline material; forming a second oxide layer on a surface of a second wafer, wherein the second wafer comprises low resistivity silicon; and, bonding the first and second oxide layers against one another so as to produce the RF semiconductor device.

In accordance with a further aspect of the present invention, a method is provided to fabricate an RF semiconductor device starting with a SOI wafer having a top silicon layer, a buried oxide layer, and a bottom

silicon layer. The method comprises the following: forming a new oxide layer on a surface of the top silicon layer; forming a high resistivity polysilicon layer over the new oxide layer; removing the bottom silicon layer of the SOI wafer; and, removing the buried oxide layer of the SOI wafer so as to produce the RF semiconductor device.

## Brief Description of the Drawings

These and other features and advantages of the present invention will become more apparent from a detailed consideration of the invention when taken in conjunction with the drawings in which:

Figure 1 illustrates is a resistance profile at the interface between the buried oxide and the substrate of a conventional Silicon-on-Insulator wafer;

Figure 2 illustrates a resistance profile across a conventional p-type wafer following standard CMOS processing;

Figure 3 illustrates an RF device that advantageously uses the present invention;

Figure 4 shows a wafer according to the present invention which may be used in the RF device of Figure 3;

Figures 5a, 5b, and 5c illustrate a process of preparing the RF substrate 20 illustrated in Figure 4;

Figures 6a, 6b, and 6c illustrate an alternative process of preparing the RF substrate 20 illustrated in Figure 4; and,

Figures 7a, 7b, 7c, 7d, and 7e illustrate a further alternative process of preparing the RF substrate 20 illustrated in Figure 4.

## Detailed Description

As shown in Figure 3, an RF device 10 incorporates an integrated circuit 12 and has an RF input 14 and an output 16. An RF substrate 20 that may be used during the fabrication of the integrated circuit 12 is shown in Figure 4. The RF substrate 20 includes a high resistivity polysilicon handle wafer 22, a buried oxide layer 24 formed over the polysilicon handle wafer 22, and a silicon layer 26 formed over the buried oxide layer 24. The silicon layer 26 of the RF substrate 20 may be then processed to form RF components, such as transistors,

capacitors, diodes, varactors, and inductors, incorporated to form the RF device 10.

The buried oxide layer 24 may be $SiO_2$ or $Al_2O_3$. Alternatively, a layer of AlN or $Si_3N_4$ may be substituted for the buried oxide layer 24. An additional layer 28 may be provided to control stress and also to reduce any warping of the RF substrate 20 and to act as a barrier layer against contamination impurities. The additional layer 28 may be provided, for example, by oxidizing the polysilicon of the polysilicon handle wafer 22 or by depositing $Si_3N_4$ on the polysilicon handle wafer 22.

The polysilicon of the polysilicon handle wafer 22 has a high resistivity $\rho$ such as a resistivity $\rho$ greater than $10^6$ $\Omega$-cm. Also, polysilicon is less susceptible to the degradation, such as type conversion, that occurs with the single crystal materials heretofore used. Moreover, high resistivity polysilicon suffers less loss of resistivity during processing.

A process of preparing the RF substrate 20 is illustrated in Figures 5a, 5b, and 5c. As shown in Figure 5a, an oxide layer 30 is formed on a surface of a first wafer 32 of single crystal silicon. This oxide layer should have the desired thickness of the buried

oxide layer 24. As shown in Figure 5b, low atomic weight atoms 34, such as hydrogen or helium atoms, may be implanted in a surface of a polycrystalline wafer 36, where the material of the polysilicon wafer 36. As shown in Figure 5c, the oxidized layer 30 of the first wafer 32 and the implanted surface of the second wafer 36 are bonded against one another, such as by use of a heat treatment. During heating, the implanted atoms form macrobubbles, and the silicon film above the implanted region is typically released. The resulting structure is the RF substrate 20 which may be polished as needed. The additional layer 28 can be added as desired.

Alternatively, as illustrated in Figures 6a, 6b, and 6c, the RF substrate 20 may be prepared by oxidizing a surface of a first wafer 40 of a polycrystalline material, such as polysilicon, to form an oxide layer 42 (Figure 6a). As shown in Figure 6b, a surface of a second wafer 44 comprising single crystal silicon is oxidized to form an oxide layer 46. As shown in Figure 6c, the oxidized layers 42 and 46 of the first and second wafers 40 and 44 are bonded together such as by use of a heat treatment. The combined depth of the oxide layers 42 and 46 should result in the desired

thickness of the buried oxide layer 24. If necessary, a portion of the exposed silicon surface of the second wafer 44 is removed such as by grinding and/or etching to produce the desired RF substrate 20 having a top silicon layer of a desired depth. If etching is used, a doped layer may be used in the single crystal wafer before bonding to stop the etching at a desired point. The additional layer 28 can be added as desired.

As a further alternative illustrated in Figures 7a, 7b, 7c, 7d, and 7e, the RF substrate 20 can be fabricated by starting with a standard SOI wafer 50 having a top silicon layer 52, a buried oxide layer 54, and a thick bottom silicon layer 56 (Figure 7a). As shown in Figure 7b, the top silicon layer 52 of the SOI wafer 50 is oxidized to form an oxide layer 58. As shown in Figure 7c, a polysilicon layer 60 is formed over the oxide layer 58 such as by deposition. The resulting polysilicon layer may have a thickness, for example, of 500 $\mu m$ for a wafer of 4 inches. As shown in Figure 7d, the thick bottom silicon layer 56 of the original SOI wafer 50 is removed, such as by etching and/or grinding. Finally, as shown in Figure 7e, the oxide layer 54 of the original SOI wafer 50 is removed, such as by etching

and/or grinding, leaving the RF substrate 20. The additional layer 28 can be added as desired.

Certain modifications of the present invention have been discussed above. Other modifications will occur to those practicing in the art of the present invention. For example, the buried oxide layers 24 and 54 described herein may be comprised of one or a combination of such dielectrics as $SiO_2$, $Si_3N_4$, $Al_2O_3$, AlN, titanates, etc. The buried oxide can be deposited using such deposition techniques as CVD, LPCVD, sputtering, MBE, PECVD, high density plasma and thermal growth.

Moreover, the other oxide layers can be selected from one or a combination of such dielectrics as $SiO_2$, $Si_3N_4$, $Al_2O_3$, AlN, titanates, etc. These other oxide layers can be deposited using such deposition techniques as CVD, LPCVD, sputtering, MBE, PECVD, high density plasma and thermal growth.

Accordingly, the description of the present invention is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the best mode of carrying out the invention. The details may be varied substantially without departing from the spirit of the invention, and the exclusive use of all

modifications which are within the scope of the appended claims is reserved.